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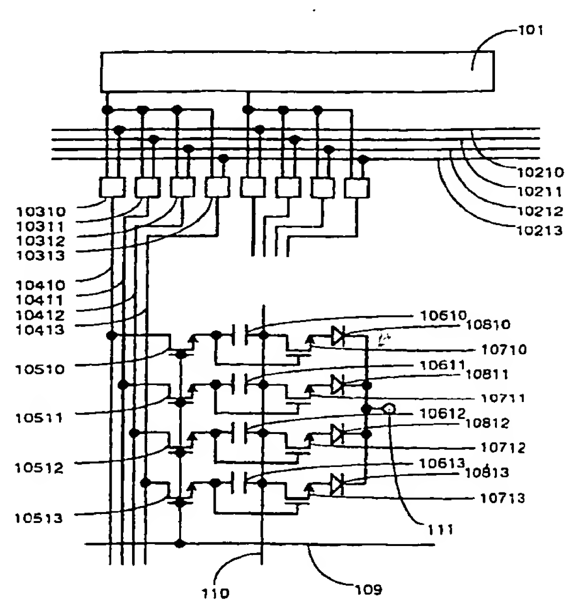
(54) DISPLAY DEVICE

(57) In a display device in accordance with the present invention, each pixel includes a plurality of luminescent elements having different luminous intensities to represent gray scales by controlling the turning ON/OFF of the luminescent elements. A digital signal is transmitted to each pixel to carry out control by thin film transistors connected in series with the luminescent elements. The luminous intensities of the luminescent elements are the geometric progressions of a common ratio of 2. The ON resistance of the thin film transistors is set to be lower than the ON resistance of the luminescent elements, while the OFF resistance of the thin film transistors is set to be higher than the OFF resistance of the luminescent elements. These features have reduced the nonuniformity in the luminous intensities of the luminescent elements caused by the nonuniformity in the conductance of the transistors, thus achieving improved image quality.

[FIG. 1]



EP 0 949 603 A1

Description

Field of the Invention

[0001] The present invention relates to a display device equipped with a display element and, more particularly, to a display device equipped with an element that emits light by means of a thin film transistor and current (hereinafter referred to as a "current luminescent display device").

Background Art

[0002] A thin film transistor organic electroluminescent device (hereinafter referred to as "TFT-OELD") may be cited as a highly promising future current luminescent display device that realizes a larger size, higher definition, a wider viewing angle, and reduced power consumption.

[0003] A method for driving a typical conventional TFT-OELD will be described.

[0004] Figure 5 shows an equivalent circuit of the conventional TFT-OELD. Only one pixel is shown in the drawing although there are actually many pixels in a plurality of rows and a plurality of columns.

[0005] A pulse is output from a shift register 101, and an analog signal of an analog signal supply line 1022 is transmitted to a source line 1042 via a transmission switch 1032. For a gate line 109 that has been selected this time, the analog signal is transmitted to a retention capacitor 1062 via a switching transistor 1052. The conductance of a current transistor 1072 is controlled in accordance with the analog signal, and an organic EL element 1082 emits light of an intensity level based on the analog signal.

[0006] Figure 6 illustrates the conventional TFT-OELD driving method.

[0007] A pulse SR0 of a shift register of a zero-th column causes an analog signal A to be transmitted to a potential S0 of a source line of a zero-th column. Further, a pulse SR1 of a shift register of a first column causes the analog signal A to be transmitted to a potential S1 of a source line of the first column. First, while a pulse G0 of a gate line of the zero-th row is being applied, the potential S0 of the source line of the zero-th column is transmitted to a potential C00 of a retention capacitor of the zero-th row and the zero-th column, whereas the potential S1 of the source line of the first column is transmitted to a potential C01 of a retention capacitor of the zero-th row and the first column. Then, while a pulse G1 of a gate line of the first row is being applied, the potential S0 of the source line of the zero-th column is transmitted to a potential C10 of a retention capacitor in the first row and the zero-th column, whereas the potential S1 of the source line of the first column is transmitted to a potential C11 of a retention capacitor in the first row and the first column. Each organic EL element 1082 (Fig. 5) emits light of a predetermined intensity level in accordance with the potential of each retention capacitor 1062 (Fig. 5), i.e., the corresponding analog signal A.

[0008] An area gray scale method is known as one of the driving methods of a liquid crystal display device. In general, a liquid crystal display device has a problem of a limited viewing angle range due to a marked change in the transmissivity or the reversal of gray scale in a direction of a viewing angle that deviates from the direction of the normal line with respect to a display surface. The foregoing area gray scale method is intended to solve the problem, and it is adapted to represent a gray scale in terms of an area ratio of full transmission to no transmission. This realizes a wider viewing angle range of a liquid crystal display device.

[0009] According to the conventional TFT-OELD driving method mentioned above, the analog signals are used to control the conductance of the current transistor 1072 so as to control the luminous intensity of the organic EL element 1082. In other words, to obtain a half tone, the conductance of the current transistor 1072 must be set to be equal to the conductance of the organic EL element 1082, and the voltage applied to the organic EL element 1082 must be controlled by dividing the voltages of the current transistor 1072 and the organic EL element 1082. In such a case, however, there has been a problem in that, if nonuniformity in the conductance of the current transistor 1072 should be produced within a panel or between panels, then the nonuniform conductance will be visually recognized in the form of nonuniform luminous intensity of the organic EL element 1082.

[0010] Accordingly, an object of the present invention is to reduce the nonuniformity in the luminous intensity of a luminescent element (an organic EL element in particular) caused by the nonuniformity in the conductance of transistors in a current luminescent display device, particularly in a TFT-OELD, thereby to improve image quality.

Disclosure of the Invention

[0011] A display device in accordance with the present invention has the following configuration.

[0012] The display device has a plurality of scanning lines, a plurality of signal lines, and a pixel formed in a matrix pattern by the scanning lines and the signal lines, a plurality of thin film transistors and a plurality of luminescent elements being formed in the pixel;

> wherein the thin film transistors and the luminescent elements are respectively connected in series, and the luminous intensities of the respective luminescent elements are different.

[0013] This permits the gray scale method to be implemented, in which each of the luminescent elements having the different luminous intensities is controlled to

be placed in either a completely ON state or a completely OFF state. With this arrangement, the nonuniformity in the luminous intensity of the luminescent elements caused by the nonuniformity in the conductance of the thin film transistors can be reduced.

[0014] In the present invention, the turning ON/OFF of the luminescent elements are preferably controlled by digital signals. This makes it possible to control each of a plurality of luminescent elements having a different luminous intensity in each pixel so as to place it in either the completely ON state or the completely OFF state.

[0015] In the present invention, the luminous intensities of the luminescent elements are preferably the geometric progressions of a common ratio of 2. This will provide each pixel with a DA converter, making it possible to obtain the luminous intensity characteristics based on digital signals.

[0016] In the present invention, it is preferable that the ON resistance of the thin film transistors is lower than the ON resistance of the luminescent elements, while the OFF resistance of the thin film transistors is higher than the OFF resistance of the luminescent elements. With this arrangement, the ON state and the OFF state of the luminescent elements can be switched by switching the ON state and the OFF state of the thin film transistors. More preferably, the ON resistance of the thin film transistors is so low that it may be ignored, as compared with the ON resistance of the luminescent elements. At this time, the current passed through the luminescent elements is determined only by the ON resistance of the luminescent elements, so that it is independent of some increase or decrease in the ON resistance of the thin film transistors. This suppresses the nonuniformity in the luminous intensity resulting from the nonuniformity of the conductance of the transistors. Further preferably, the OFF resistance of the thin film transistors is far higher than the OFF resistance of the luminescent elements. Thus, the luminescent elements can be securely placed in the OFF state.

[0017] In the present invention, the thin film transistors are preferably polycrystalline silicon thin film transistors produced at a low temperature process at 600 degrees Celsius or lower. This makes it possible to implement larger areas at low cost and also to achieve such features as high mobility for enabling the luminescent elements to be driven and high reliability.

[0018] In the present invention, the luminescent elements are preferably organic electroluminescent elements produced by an ink-jet process. With this arrangement, it is possible to pattern an organic electroluminescent element, which achieves outstanding characteristics including high luminous efficiency and long service life, on a panel.

Brief Description of the Drawings

[0019]

Fig. 1 is an equivalent circuit diagram of a TFT-OELD of a first embodiment in accordance with the present invention.

Fig. 2 provides a top plan view and a sectional view of the TFT-OELD of the first embodiment in accordance with the present invention.

Fig. 3 is a view showing a driving method for the TFT-OELD of the first embodiment in accordance with the present invention.

Fig. 4 is an equivalent circuit diagram of a TFT-OELD of a second embodiment in accordance with the present invention.

Fig. 5 is an equivalent circuit of a conventional TFT-OELD.

Fig. 6 is a diagram illustrative of a driving method for the conventional TFT-OELD.

Description of Reference Numerals

[0020]

101	Shift register
10210	Zero-th bit digital signal supply line
10211	First-bit digital signal supply line
10212	Second-bit digital signal supply line
10213	Third-bit digital signal supply line
1022	Analog signal supply line
10310	Zero-th bit transmission switch
10311	First-bit transmission switch
10312	Second-bit transmission switch
10313	Third-bit transmission switch
1032	Transmission switch
10410	Zero-th bit source line
10411	First-bit source line
10412	Second-bit source line
10413	Third-bit source line
1042	Source line
10510	Zero-th bit switching transistor
10511	First-bit switching transistor
10512	Second-bit switching transistor
10513	Third-bit switching transistor
1052	Switching transistor
10610	Zero-th bit retention capacitor
10611	First-bit retention capacitor
10612	Second-bit retention capacitor
10613	Third-bit retention capacitor
1062	Retention capacitor
10710	Zero-th bit current transistor
10711	First-bit current transistor
10712	Second-bit current transistor
10713	Third-bit current transistor
1072	Current Transistor
10810	Zero-th bit organic EL element
10811	First-bit organic EL element

10812	Second-bit organic EL element
10813	Third-bit organic EL element
1082	Organic EL element
109	Gate line
1090	Gate line for lower-order bits
1091	Gate line for higher-order bits
110	Common electrode
111	Upper electrode
SR0	Pulse of shift register of zero-th column
SR1	Pulse of shift register of first column
D0	Zero-th bit digital signal
D1	First-bit digital signal
A	Analog signal
S00	Potential of source line of zero-th column and zero-th bit
S01	Potential of source line of zero-th column and first bit
S10	Potential of source line of first column and zero-th bit
S11	Potential of source line of first column and first bit
S0	Potential of source line of zero-th column
S1	Potential of source line of first column
G0	Pulse of gate line of zero-th row
G1	Pulse of gate line of first row
C000	Potential of retention capacitor of zero-th row, zero-th column, and zero-th bit
C001	Potential of retention capacitor of zero-th row, zero-th column, and first bit
C010	Potential of retention capacitor of zero-th row, first column, and zero-th bit
C011	Potential of retention capacitor of zero-th row, first column, and first bit
C100	Potential of retention capacitor of first row, Zero-th column, and zero-th bit
C101	Potential of retention capacitor of first row, zero-th column, and first bit
C110	Potential of retention capacitor of first row, first column, and zero-th bit
C111	Potential of retention capacitor of first row, first column, and first bit
C00	Potential of retention capacitor of zero-th row and zero-th column
C01	Potential of retention capacitor of zero-th row and first column
C10	Potential of retention capacitor of first row and zero-th column
C11	Potential of retention capacitor of first row and first column

Best Mode for Carrying Out the Invention

[0021] Embodiments of the present invention will be described with reference to the accompanying drawings.

(First Embodiment)

[0022]

Figure 1 is an equivalent circuit diagram of a TFT-OELD of a first embodiment in accordance with the present invention. Although only one pixel is shown in the drawing, there are many pixels arranged in a plurality of rows and a plurality of columns in an actual device.

When a pulse is output from a shift register 101, digital signals of digital signal supply lines 10210 through 10213 of zero-th through third bits are transmitted to source lines 10410 through 10413 via transmission switches 10310 through 10313 of the zero-th through third bits. In other words, the digital signals are transmitted to each pixel. For a gate line 109 that has been selected at this time, the digital signals are respectively transmitted to retention capacitors 10610 through 10613 of the zero-th through third bits via switching transistors 10510 through 10513 of the zero-th through third bits, respectively. Current transistors 10710 through 10713, which are thin film transistors, and organic EL elements 10810 through 10813, which are current elements, are respectively connected in series. Hence, the ON/OFF control of the current transistors 10710 through 10713 of the zero-th through third bits are conducted by the digital signals so that the organic EL elements 10810 through 10813 of the zero-th through third bits emit light or emit no light in response to the digital signals.

Figure 2 provides a top plan view and a sectional view of the TFT-OELD of the first embodiment in accordance with the present invention.

The organic EL elements 10810 through 10813 of the zero-th through third bits, which are luminescent elements, have different areas to provide different luminous intensity levels, permitting the so-called area gray scale method to be implemented. In addition, the areas or the luminous intensities are set to the geometric progressions of a common ratio of 2 so as to provide each pixel with a DA converter.

In this embodiment, polycrystalline silicon thin film transistors that have been produced at a low-temperature process of 600 degrees Celsius or below are used as the thin film transistors making up the shift register 101, the transmission switches 10310 through 10313 of the zero-th through third bits, the switching transistors 10510 through 10513 of the zero-th through third bits, and the current transistors 10710 through 10713, etc.; however, other elements may be used as long as they have equivalent functions. The organic semiconductor films constituting the organic EL elements 10810 through 10813 of the zero-th through third bits are formed using the so-called ink-jet process in which

a liquid material is discharged from an ink-jet head; however, current luminescent elements formed by a different process or current luminescent elements other than the organic EL elements may be employed instead.

Figure 3 illustrates the driving method of the TFT-OELD of the first embodiment in accordance with the present invention.

A pulse SR0 of a shift register of a zero-th column causes digital signals D0 and D1 of the zero-th and first bits to be transmitted to potentials S00 and S01 of source lines of the zero-th and first bits in the zero-th column. Further, a pulse SR1 of a shift register of a first column causes the digital signals D0 and D1 of the zero-th and first bits to be transmitted to potentials S10 and S11 of source lines of the zero-th and first bits in the first column. While a pulse G0 of a gate line of the zero-th row is being applied, potentials S00 and S01 of source lines of the zero-th and first bits in the zero-th column are transmitted to potentials C000 and C001 of retention capacitors of the zero-th and first bits in the zero-th row and the zero-th column, while potentials S10 and S11 of source lines of the zero-th and first bits in the first column are transmitted to potentials C010 and C011 of retention capacitors of the zero-th and first bits in the zero-th row and the zero-th column. Then, while a pulse of a first-row gate line is being applied, potentials S00 and S01 of the source lines of the zero-th and first bits in the zero-th column are transmitted to potentials C100 and C101 of retention capacitors of the zero-th and first bits in the first row and the zero-th column, while potentials S10 and S11 of the source lines of the zero-th and first bits in the first column are transmitted to potentials C110 and C111 of retention capacitors of the zero-th and first bits in the first row and the first column. The respective organic EL elements emit light or emit no light in accordance with the potentials of the respective retention capacitors, i.e., the corresponding digital signals.

In this case, the resistance of the current transistors in the ON state is sufficiently small to be ignored as compared with that of the organic EL elements in the ON state. Hence, the current passing through the organic EL elements depends only on the resistance of the organic EL elements with respect to the voltage between a common electrode 110 and an upper electrode 111, and it is independent from some increase or decrease in the resistance of the current transistors. Hence, the nonuniformity in the luminous intensity caused by the nonuniformity in the conductance of the transistors can be suppressed. Further, the resistance of the current transistors in the OFF state is substantially higher than the resistance of the organic EL elements in the OFF state. This makes it possible to securely put the organic EL elements in the OFF state.

(Second Example)

[0023]

Figure 4 is an equivalent circuit diagram of a TFT-OELD of a second embodiment in accordance with the present invention.

The operations, functions, and advantages of the TFT-OELD of this embodiment are almost identical to those of the first embodiment. In this embodiment, however, a gate line 109 is divided into a gate line 1090 for lower-order bits that is assigned the functions of zero-th and first bits and a gate line 1091 for higher-order bits that is assigned the functions of second and third bits. This makes it possible to reduce the number of digital supply lines and the number of transmission switches and source lines per column from four to two. However, the frequencies of the scanning signals of the gate lines, the pulses of the shift register, and the digital signals will be doubled.

(Application Example)

[0024] The present invention is intended to reduce the nonuniformity in the luminous intensity of luminescent elements caused by the nonuniformity in the conductance of transistors in a current luminescent display element and therefore it is intrinsically different from the area gray scale method of the liquid crystal display element mentioned in "Background Art." In fact, current luminescent display elements do not even need to have different areas as long as they have different luminous intensity levels. Their structures, however, have similar aspects. Therefore, many embodiments disclosed in relation to the area gray scale method of liquid crystal display elements can be applied to the gray scale method in accordance with the present invention, and similar advantages to those of the disclosed embodiments can be expected.

Industrial Applicability

[0025] Having the advantages described above, the present invention is ideally used with a display device equipped with elements that emit light by means of thin film transistors and current. As the light emitting elements, organic electroluminescent elements, for example, can be used. Further, a display device to which the present invention has been applied can be used not only for a personal computer for personal use, and a portable electronic pocketbook but also for information display equipment including an outdoor large bulletin board and an advertisement signboard.

Claims

1. A display element comprising a plurality of scanning lines, a plurality of signal lines, and a pixel formed in a matrix pattern by the scanning lines and the signal lines, a plurality of thin film transistors and a plurality of luminescent elements being formed in the pixel;

   wherein the thin film transistors and the luminescent elements are respectively connected in series, and the luminous intensities of the respective luminescent elements are different.

2. A display device according to Claim 1, wherein the turning ON/OFF of the luminescent elements is controlled by a digital signal.

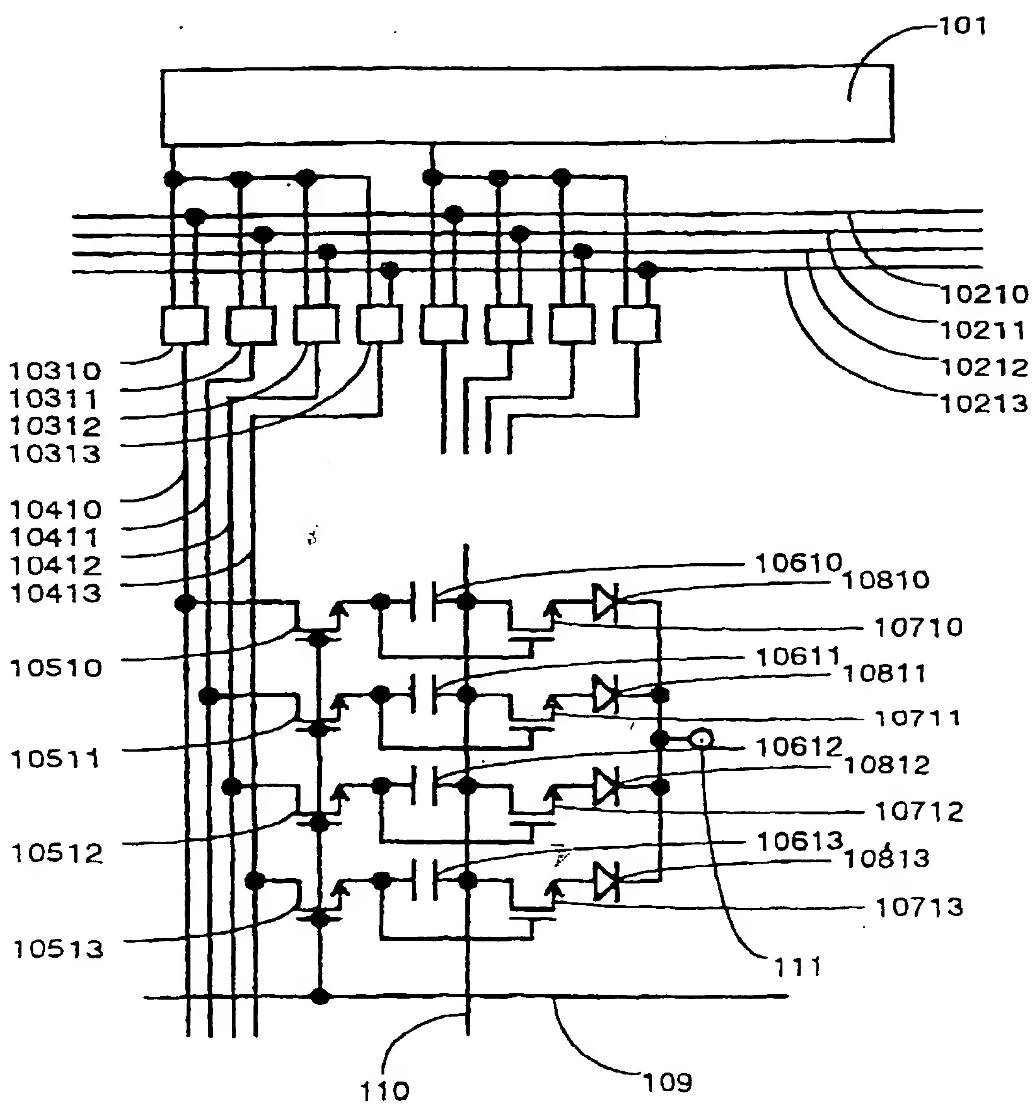
3. A display device according to Claim 1, wherein luminous intensities of the luminescent elements are geometric progressions of a common ratio of 2.

4. A display device according to Claim 1, wherein ON resistance of the thin film transistors is lower than ON resistance of the luminescent elements, while OFF resistance of the thin film transistors is higher than the OFF resistance of the luminescent elements.

5. A display device according to Claim 1, wherein the thin film transistors are polycrystalline silicon thin film transistors produced at a low temperature process at 600 degrees Celsius or below.

6. A display device according to Claim 1, wherein the luminescent elements are organic electroluminescent elements produced by an ink-jet process.

[FIG. 1]


101
10210
10211
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10310
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10411
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10413
10610
10810
10710
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10711
10612
10812
10511
10712
10613
10813
10512
10713
10513
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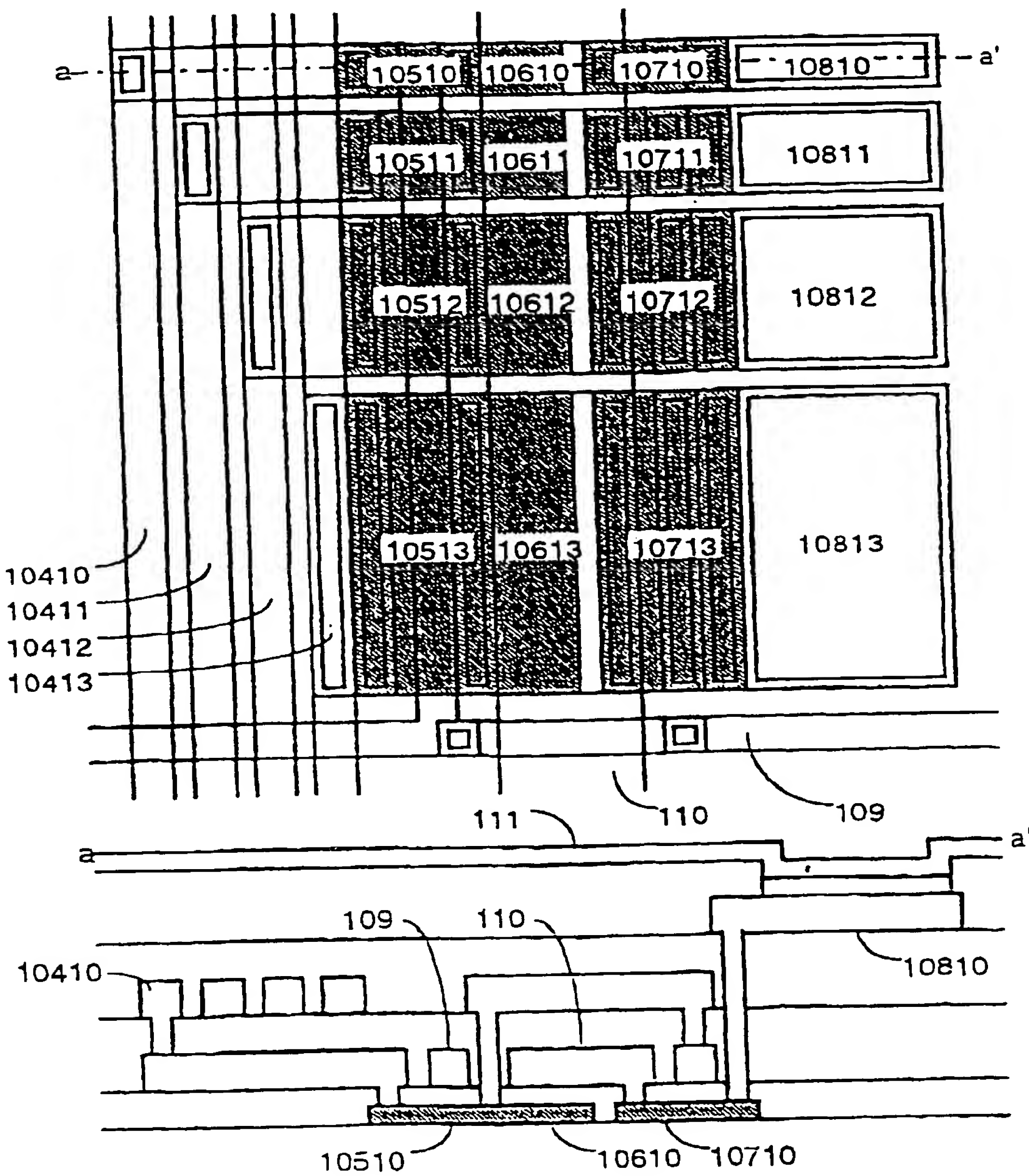
[FIG. 2]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a'
10510
10610
10710
10810
10511
10611
10711
10811
10512
10612
10712
10812
10513
10613
10713
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10410
10411
10412
10413
111
110
109
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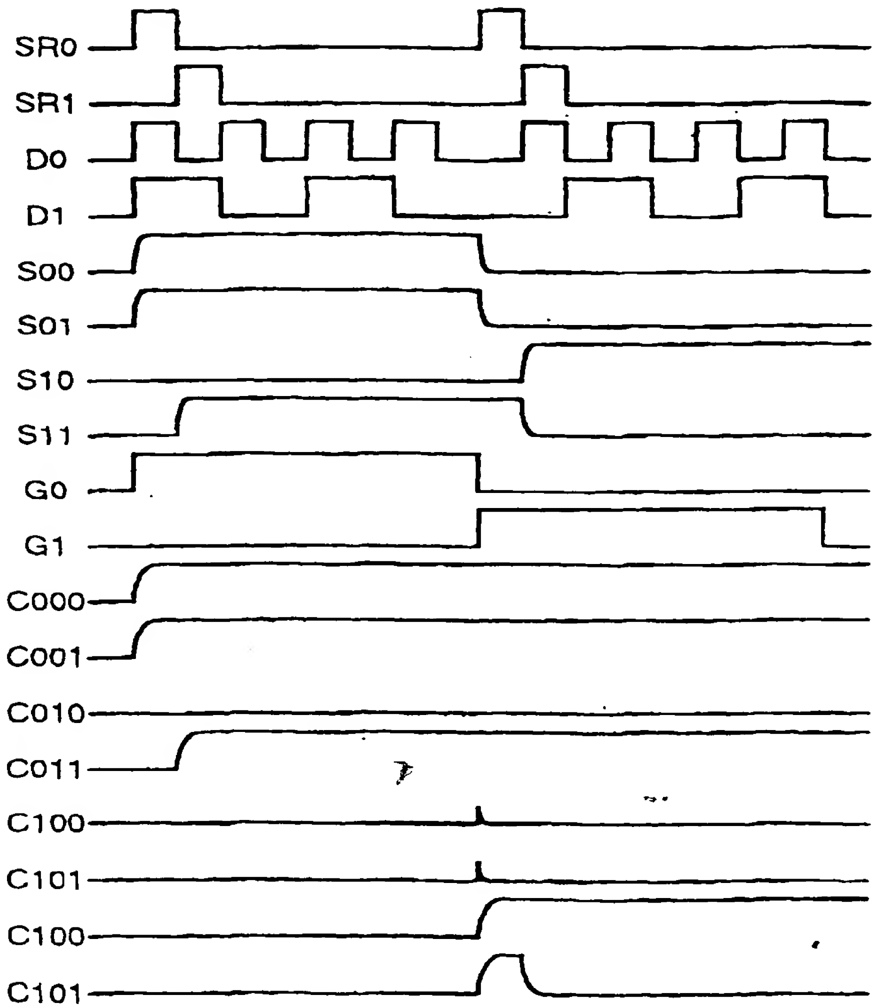
a'
109
110
10410
10810
10510
10610
10710

[FIG. 3]


SR0
SR1
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S01
S10
S11
G0
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C000
C001
C010
C011
C100
C101
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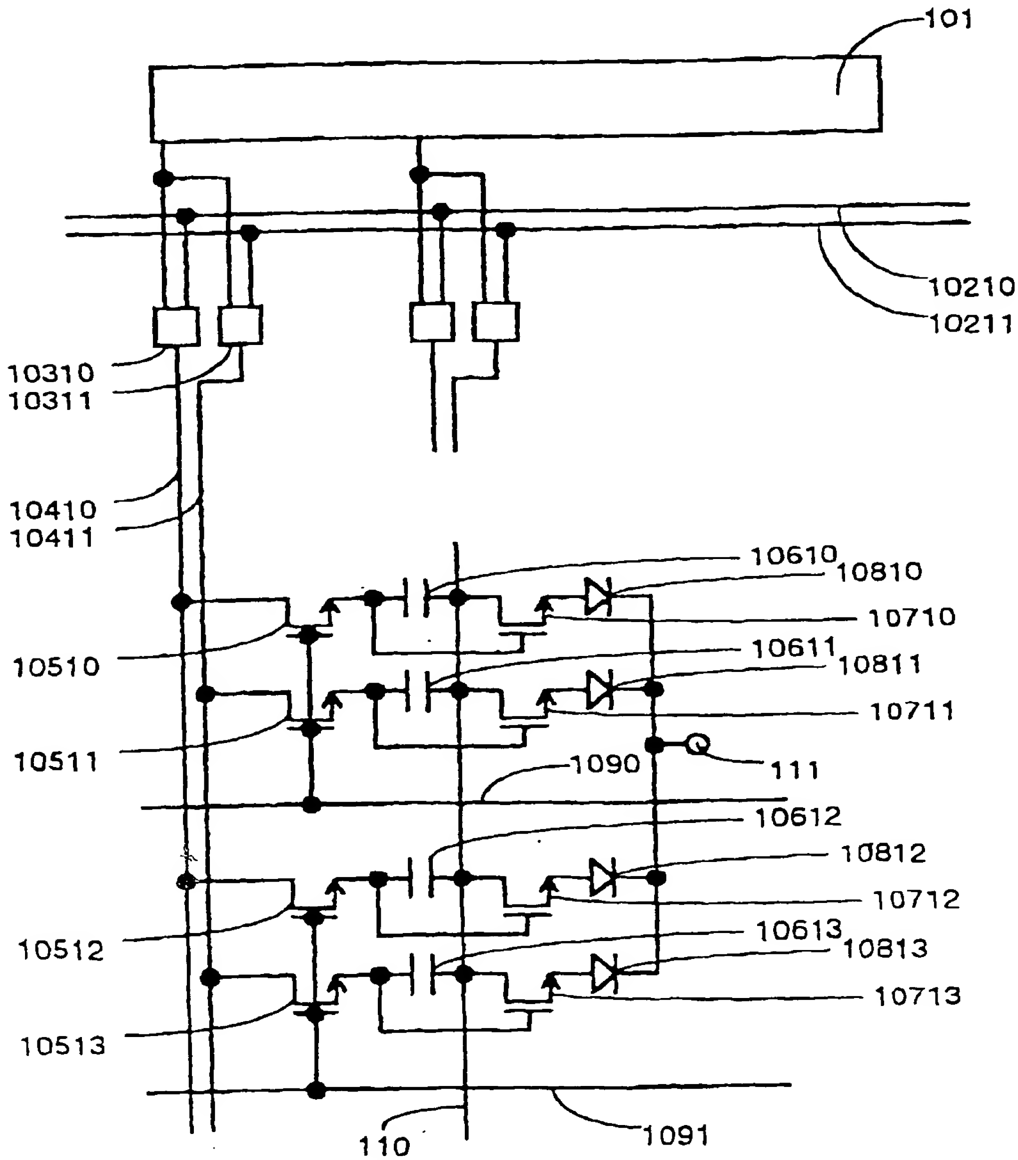
[FIG. 4]


101
10210
10211
10310
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10410
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10610
10810
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10711
10511
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111
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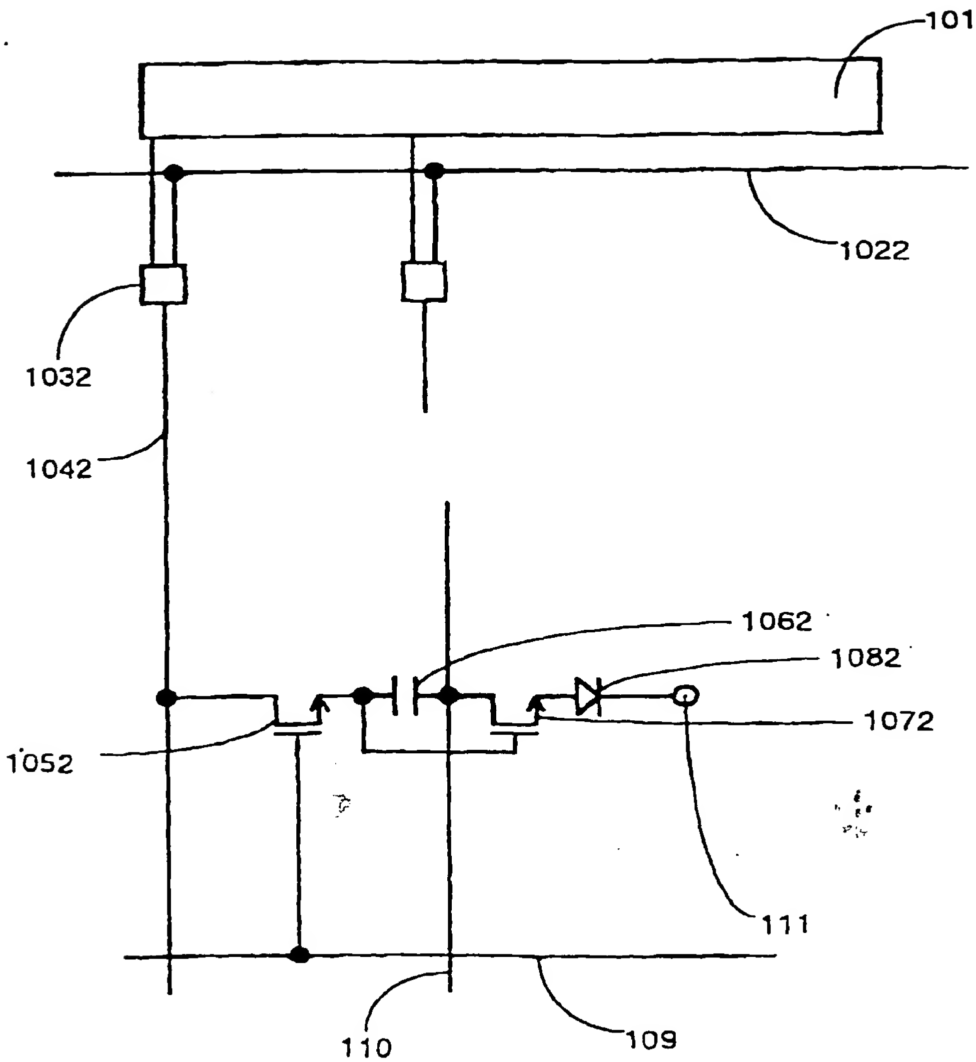
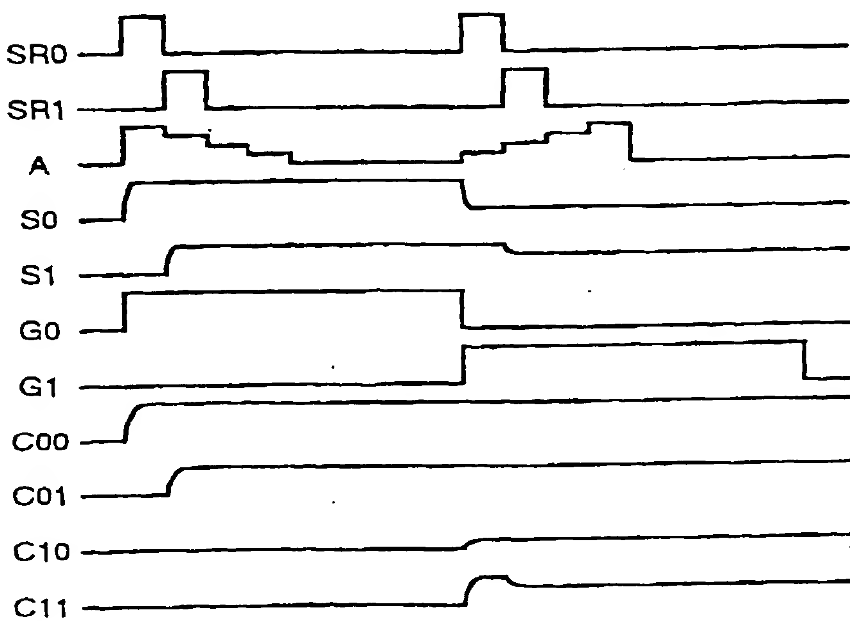
[FIG. 5]



[FIG. 6]



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP98/03756

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl^6 G09G3/30, G09F9/30, H05B33/26, H05B33/10

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl^6 G09G3/00-3/38, G09F9/30-9/46, H05B33/00-33/28

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1926-1996 Toroku Jitsuyo Shinan Koho 1994-1998
Kokai Jitsuyo Shinan Koho 1971-1995

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP, 61-22326, A (Citizen Watch Co., Ltd.), 30 January, 1986 (30. 01. 86) (Family: none)	1-6
Y	JP, 56-88193, A (Citizen Watch Co., Ltd.), 17 July, 1981 (17. 07. 81) (Family: none)	1-6
Y	JP, 58-220185, A (Daini Seikosha K.K.), 21 December, 1983 (21. 12. 83) (Family: none)	1-6
Y	JP, 8-54835, A (NEC Corp.), 27 February, 1996 (27. 02. 96) & US, 5714968, A	1-6
Y	JP, 6-325869, A (Mitsubishi Kasei Corp.), 25 November, 1994 (25. 11. 94) (Family: none)	1-6
Y	JP, 8-241057, A (TDK Corp., Semiconductor Energy Laboratory Co., Ltd.), 17 September, 1996 (17. 09. 96) & US, 5786796, A	4

[x] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

* Special categories of cited documents:
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Date of the actual completion of the international search	Date of mailing of the international search report
1 December, 1998 (01. 12. 98)	8 December, 1998 (08. 12. 98)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP98/03756

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP, 9-153524, A (Sony Corp.), 10 June, 1997 (10. 06. 97) (Family: none)	5
Y	JP, 7-235378, A (Casio Computer Co., Ltd.), 5 September, 1995 (05. 09. 95) (Family: none)	6

Form PCT/ISA/210 (continuation of second sheet) (July 1992)